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EXAMINER

SCHLICHTER, ANDREW M

ART UNIT

PAPER NUMBER

2871

MAIL DATE

DELIVERY MODE

06/18/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/082,984

**Applicant(s)**

KONISHI ET AL.

**Examiner**

ANDREW SCHECHTER

**Art Unit**

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 March 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 11 March 2008 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The applicant argues [pp. 4-5] that *Song* discloses in Fig. 12 a pixel electrode [40] and not a terminal electrode. This is not persuasive. In Fig. 12, *Song* discloses both a pixel electrode [40 in the "C" region"] and a terminal electrode [40 in the "D" region], as clearly pointed out in the rejection. Region D is clearly identified in *Song* as the region where the pads (or terminals) are formed [col. 4, lines 9-14, for instance], which is the region outside the display area at the periphery of the device. The applicant argues [p. 5] that pad region D is actually the display area, but this is simply wrong, with the confusion caused no doubt by the use of "40" to label both the pixel electrode and the terminal electrode in the figure. They are both labeled with the same identifier because they are formed of the same layer at the same time, but they are not electrically connected with each other (clearly the "40" in region D cannot be a pixel electrode since it would be short-circuited to gate pads, making the device non-functional). The examiner suggests that a comparison of *Song* with the *Takizawa* and *Lee* references could help alleviate this confusion.

The previous rejections are therefore repeated below, modified as necessary by the amendments to the claims.

***Claim Objections***

2. Claim 1 is objected to because of the following informalities: "the drain electrode" in the third-to-last line should be "a drain electrode". Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Song et al.*, U.S. Patent No. 5,851,918 in view of *Takizawa et al.*, U.S. Patent No. 5,742,074 and further in view of *Lee et al.*, U.S. Patent No. 6,587,160.

*Song* discloses [see Fig. 12, for instance] a liquid crystal display comprising a TFT substrate [22, etc.], wherein the TFT array substrate has a display area ["C"] and a terminal forming area ["D"], the display area is provided with a pixel electrode [40 in the "C" region], a switching element [24, 30, 34, etc.] connected to the pixel electrode, the terminal forming area is provided with a terminal electrode [40 in the "D" region], and wherein a first metallic line [34c, made of chromium, col. 5, lines 43-44] and a second metallic line [24a, made of aluminum, col. 5, lines 18-19], both connected to the terminal electrode via respective contact holes [the holes in passivation layer 36], are arranged below the terminal electrode at the terminal forming area, and an insulating layer [28] is

interposed between the first metallic line and the second metallic line [note that, as shown in the applicant's own Figs. 2 and 3, the first and second metallic lines do not need to overlap each other in order for the insulating layer to be "interposed between" them].

*Song* is silent on, and therefore does not explicitly disclose, the following conventional details of LCDs: a counter substrate facing the TFT substrate and liquid crystal interposed between the substrates, a gate line connected to the switching element and a source line connected to the switching element, source and drain electrodes in the same layer, and the terminal electrode being for connecting the gate line or source line to at least one external signal source. *Takizawa* discloses an analogous LCD, with analogous display and terminal forming areas [see Fig. 1 or 24, for instance], and explicitly discloses a counter substrate facing the TFT substrate and liquid crystal interposed between the substrates [col. 8, lines 60-65], a gate line [14] connected to the analogous switching element [40] and a source line [16] connected to the switching element [see Fig. 3, for instance], source and drain electrodes in the same layer, and the terminal electrode being for connecting the gate line or source line to at least one external signal source [col. 7, lines 25-30, for instance]. It would have been obvious to one of ordinary skill in the art to have these conventional features in the device of *Song*, motivated by the desire to form a functioning LCD with a liquid crystal and counter substrate, to have an active matrix of gate and data lines to produce an image from an array of pixels, and to provide the external signals which direct what image is to be formed, respectively.

*Song* also is silent on, and therefore does not explicitly disclose, that the insulating layer serves, during fabrication of said display, to minimize exfoliation of the second metallic line, and short circuits resulting from such exfoliation. However, the structure recited in the reference is substantially identical to that of the claim [each has two metallic lines, formed of the same gate and source line layers, which are separated by a gate insulating layer made of silicon nitride]. In such situations, claimed properties or functions [such as serving to minimize exfoliation of one of the metallic lines during fabrication] are presumed to be inherent [see MPEP 2112.01]. Alternatively, this limitation could be considered a product-by-process limitation [the product is made by a process which includes a step in which the insulating layer serves to minimize exfoliation]. In such situations, the claim is not limited by the manipulations of the recited steps, but only by the structure implied by the steps [see MPEP 2113]. Here, the only structure implied is having a relatively low number of exfoliations and short circuits, which is not a patentable distinction as this would have been obvious to one of ordinary skill in the art at the time of the invention motivated by the desire to avoid such defects. So, the burden shifts to the applicant to show an unobvious difference between the prior art and the claimed invention [see MPEP 2113].

Considering the limitations amended to claim 1 on 11 March 2008, *Song* does not appear to explicitly disclose that a side of the substrate (on the other side of the terminals from the display area) is cut off during the fabrication of the LCD). However, *Lee* discloses [see Figs. 3 and 14, for instance] an analogous device to that of *Song* [compare Fig. 14 to Fig. 12 of *Song*, for instance], in which there is explicitly shown a

shorting bar [102] and a cutting line [11] on the other side of the terminals from the display area. It would have been obvious to one of ordinary skill in the art to cut off the substrate during fabrication of *Song's* device as shown in *Lee*, motivated by the desire to have a shorting bar to prevent electrostatic charge damage during the fabrication, and the desire to remove the shorting bar so that the signal lines are not shorted to each other during use, as well as getting rid of excess unused peripheral areas to make the display more compact.

The above device therefore has the first metallic line [34c] and the second metallic line [24a] being made from different metallic layers in a first side of the terminal forming area facing the display area [where 24a is] and in a second side of the terminal forming area facing the side where the substrate is cut off during fabrication of the LCD [where 34c is], the first metallic line [34c] below the terminal electrode is the source line which is made from the metal film for the source electrode and the drain electrode [the source line shown in *Takizawa* would be an extension of the source electrode 34a of *Song*], and the second metallic line [24a] below the terminal electrode is the supplementary line which is made from the metal film for the gate line [the gate line shown in *Takizawa* would be an extension of the gate electrode 24 of *Song*].

Claim 1 is therefore unpatentable.

*Song* in view of *Takizawa* also has the first metallic line [34c] made from the same layer as that for the source line [the source line shown in *Takizawa* would be an extension of the source electrode 34a of *Song*] and has the second metallic line [24a] made from the same layer as that for the gate line [the gate line shown in *Takizawa*

would be an extension of the gate electrode 24 of *Song*], so claim 2 is also unpatentable.

Considering claims 3 and 4, *Song* also discloses that the second metallic line [24a] is arranged in a lower layer than the first metallic line [34c]. *Song* does not explicitly disclose that the first metallic line is connected to the source line. However, the purpose of these terminal structures is to be connected to such lines, as can be seen in the analogous LCD shown in Figs. 24-32 of *Takizawa* [this is the fourth embodiment, which discloses, like *Song*, electrodes connected via respective contact holes to two lines below them, see Fig. 28D in particular]. Considering the source lines and source terminals in Figs. 28D and 32, for instance, the electrodes [35] are analogous to the terminal electrodes [40] in *Song*, being connected through one contact hole to a lower electrode [34b, like the second metallic line in *Song*] and through another contact hole to a slightly higher electrode [36b, like the first metallic line in *Song*], which is connected to the source line [16b]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first metallic line in *Song* connected to the source line, motivated by the desire to use the terminal structure in *Song* to provide for electrical connection to the source lines. Claims 3 and 4 are therefore unpatentable.

Considering claims 5 and 6, *Song* also discloses that the second metallic line [24a] is arranged in a lower layer than the first metallic line [34c]. *Song* does not explicitly disclose that the second metallic line is connected to the gate line. However, the purpose of these terminal structures is to be connected to such lines, as can be

seen in the analogous LCD shown in Figs. 24-32 of *Takizawa* [this is the fourth embodiment, which discloses, like *Song*, electrodes connected via respective contact holes to two lines below them, see Fig. 28D in particular]. Considering the gate lines and gate terminals in Figs. 28D and 32, for instance, the electrodes [25] are analogous to the terminal electrodes [40] in *Song*, being connected through one contact hole to a lower electrode [24a, like the first metallic line in *Song*] and through another contact hole to an even lower electrode [26a, like the second metallic line in *Song*], which is connected to the gate line [14a]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first metallic line in *Song* connected to the gate line, motivated by the desire to use the terminal structure in *Song* to provide for electrical connection to the gate lines. Claims 5 and 6 are therefore unpatentable.

Note that in claims 3 and 4 the recited terminal electrode is connected to a source line, and in claims 5 and 6 the recited terminal electrode is connected to a gate line. The rejection above should therefore be understood to refer to two separate terminal electrodes in the device of *Song* in view of *Takizawa*, one on the source side of the display for claims 3 and 4, and one on the gate side of the display for claims 5 and 6, rather than a single terminal electrode satisfying all four claims.

### ***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2871

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/  
Primary Examiner, Art Unit 2871  
Technology Center 2800  
16 June 2008